(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 697 792 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
21.02.1996 Bulletin 1996/08

(51) Int Cl.[6]: **H04N 5/92**, H04N 7/30

(21) Application number: **95305784.1**

(22) Date of filing: **18.08.1995**

(84) Designated Contracting States:
AT DE FR GB IT NL

(30) Priority: **19.08.1994 JP 195230/94**

(71) Applicant: **SONY CORPORATION**
Tokyo 141 (JP)

(72) Inventors:
- **Oikawa, Yuka, c/o Int. Prop. Div. Sony Corp.**
  Shinagawa-ku, Tokyo 141 (JP)
- **Yanagihara, Naofumi,**
  c/o Int. Prop. Div. Sony Corp
  Shinagawa-ku, Tokyo 141 (JP)
- **Izumi, Nobuaki, c/o Int. Prop. Div. Sony Corp**
  Shinagawa-ku, Tokyo 141 (JP)

(74) Representative: **Cotter, Ivan John et al**
London EC4A 1DA (GB)

(54) Recording digital video signals

(57) In a technique for recording digital video signals, digital video signals in the form of DCT coefficients, obtained by e.g. discrete cosine transformation, are quantized and compressed so as to be recorded on a recording medium. A first quantization step decision unit (23) determines a quantization step in terms of a video segment made up of plural macro-blocks as a unit so that the quantity of quantized data is less than a pre-set data quantity. A second quantization step decision unit (24) determines a quantization step in terms of the macro-blocks as a unit so that the quantity of quantized data is less than the pre-set data quantity. A quantization unit (25) quantizes the digital video signals with quantization steps determined by the first and second quantization step decision units (23, 24). This enables efficient encoding and improved picture quality.

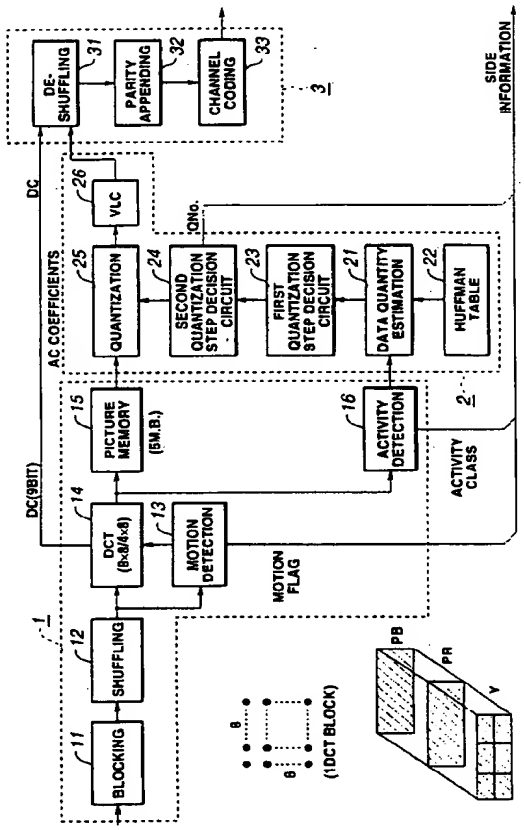


FIG.1

EP 0 697 792 A2

Description

This invention relates to methods of and apparatus for processing digital video signals, in which the digital video signals, which may for instance be in the form of DCT coefficients, obtained by, for example, a discrete cosine transform operation, are quantized and compressed, for example for recording on a recording medium. More particularly, but not exclusively, the invention relates to methods and apparatus for recording digital video signals which advantageously may be employed for a digital video tape recorder for recording/reproducing video signals for a high definition television system.

For background information pertinent to the present application, the reader is referred to our US Patents Nos. US-A-5 321 440 and US-A-5 317 413 and to our Japanese Patent Applications Nos. 03-317497 (filed 5 November 1991), 04-196219 (filed 30 June 1992), 04-213716 (filed 17 July 1992), 04-181577 (filed 17 June 1992) and 05-223226 (filed 8 September 1993). Each of the above patents and applications is hereby incorporated herein by reference.

In recent years, developments of a digital video tape. recorder in which video signals are converted into digital signals and encoded using a high efficiency encoding system such as discrete cosine transform (DCT) and the resulting encoded data is recorded and/or reproduced on or from a magnetic tape using a rotary head, are proceeding briskly.

The digital VTR may be set to a mode for recording video signals of the current television system, such as the NTSC system, referred to herein as a SD mode, or to a mode for recording video signals of the high definition television system, referred to herein as a HD mode.

By the recording system of the above-mentioned digital VTR, the video signals are compressed and recorded as digital video signals of approximately 25 Mbps and as digital video signals of approximately 50 Mbps for the SD mode and for the HD mode, respectively.

In the method for recording the digital video signals in the above-mentioned recording system, the video signal, converted into the digital signals, are divided into blocks of a suitable size, such as DCT blocks of 8x8 pixels. Six DCT blocks of luminance data, one DCT block of R-Y data and one DCT block of B-Y data, totalling eight blocks, make up one macro-block.

A plurality of macro-blocks are shuffled, that is, five macro-blocks at discrete positions on a picture are assembled into one unit. Two-dimensional DCT is then carried out on the unit basis, with the block size of 8 x 8.

Data obtained by the two-dimensional DCT, that is DCT coefficients, are stored in a memory on the unit basis. The total number of codes are estimated on the unit basis and the quantization steps are determined which will give the total number of codes which is smaller than a pre-set value.

The DCT coefficients are then quantized on the unit basis, with the thus determined quantization step, and variable length encoded by the Huffman code. The resulting quantized units are accommodated in video segments by way of framing.

The codes thus quantized and accommodated in a fixed bit length range on the unit basis, that is on the video segment basis, are re-arrayed in a sequence in which the macro-blocks are arrayed in continuous sequence on the picture, so as to be recorded at pre-set positions on the magnetic tape.

With the above-described recording method for the digital video signals, a sole quantization step is accorded to each video segment and all DCT coefficients in each video segment are quantized with the thus accorded quantization step. That is, the same quantization step is accorded to plural macro-blocks. Thus the quantization step is determined so that the total number of quantized codes on setting the fixed bit length on the video segment basis will be less than a pre-set value. However, it is a frequent occurrence that the actual mount of quantized codes on fixed length coding becomes significantly smaller than the above-mentioned pre-set value, so that efficient encoding cannot be achieved. On the other hand, the degree of quantization for the respective blocks becomes coarse with the result that the picture cannot be improved in quality.

According to the present invention there is provided a method for recording quantized and encoded digital video signals comprising the steps of determining a quantization step in terms of a video segment made up of plural macro-blocks as a unit so that the quantity of quantized data is less than a pre-set data quantity, determining a quantization step in terms of the macro-blocks as a unit so that the quantity of quantized data is less than the pre-set data quantity, and quantizing the digital video signals with the determined quantization steps.

With an embodiment, described hereinbelow, of the above method for recording digital video signals, the quantization step is determined on the macro-block basis by giving priority to the macro-block which is located at a mid portion of a picture.

According to the present invention there is also provided an apparatus for recording quantized and encoded digital video signals comprising first quantization step decision means for determining a quantization step in terms of a video segment made up of plural macro-blocks as a unit so that the quantity of quantized data is less than a pre-set data quantity, second quantization step decision means for determining a quantization step in terms of the macro-blocks as a unit so that the quantity of quantized data is less than the pre-set data quantity, and quantization means for quantizing the digital video signals with the quantization steps determined by the first quantization step decision means and the

second quantization step decision means.

With an embodiment, described hereinbelow, of the above apparatus for recording digital video signals, the quantization step is determined on the macro-block basis by giving priority to the macro-block which is located at a mid portion of a picture.

With the embodiment, described hereinbelow, of the above method for recording digital video signals, a quantization step is determined in terms of the macro-blocks as a unit so that the quantity of quantized data is less than a pre-set data quantity. On the other hand, a quantization step is also determined in terms of the macro-blocks as a unit so that the quantity of quantized data is less than the pre-set data quantity. The digital video signals are quantized with the quantization steps thus determined and the quantized and encoded digital video signals are recorded on a recording medium. This enables the degree of quantization to be refined in a range of a pre-set data quantity of the quantized data to render it possible to make effective utilization of redundant bits, thus assuring efficient encoding and improved picture quality.

With the embodiment, described below, of the above method for recording digital video signals, since the quantization step is determined on the macro-block basis by giving priority to the macro-block which is located at a mid portion of a picture, the picture of satisfactory quality can be obtained in a mid portion of the picture which may be noticed most readily by the eye, thus further assuring improved picture quality.

With the embodiment, described below, of the above apparatus for recording digital video signals, the first quantization step decision unit determines a quantization step in terms of a video segment made up of plural macro-blocks as a unit so that the quantity of quantized data is less than a pre-set data quantity, while the second quantization unit decision unit determines a quantization step in terms of the macro-blocks as a unit so that the quantity of quantized data is less than the pre-set data quantity. The quantization unit quantizes the digital video signals with the quantization steps determined by the first quantization step decision unit and the second quantization step decision unit. This enables the degree of quantization to be refined in a range of a pre-set data quantity of quantized data to render it possible to make effective utilization of redundant bits, thus assuring efficient encoding and improved picture quality.

With the embodiment, described below, of the above apparatus for recording digital video signals, since the quantization step is determined on the macro-block basis by giving priority to the macro-block which is located at a mid portion of a picture, the picture of satisfactory picture quality can be obtained in a mid portion of the picture which may be noticed most readily by the eye, thus further assuring improved picture quality.

The embodiment of the present invention described below provides a method and apparatus for digital video signals in which the quantization step determined on the video segment basis is shifted on the macro-block basis so that the quantization steps will be determined on the macro-block basis for enabling efficient encoding and improving the picture quality.

The invention will now be further described, by way of illustrative and non-limiting example, with reference to the accompanying drawings, in which:

Fig.1 is a block diagram showing an arrangement of an encoder of a recording apparatus for digital video signals for carrying out a digital video signal recording method according to an embodiment of the present invention.

Fig.2 illustrates a shuffling operation for five macro-blocks.

Fig.3 illustrates the order of scanning in a super-block in the shuffling operation.

Fig.4 illustrates the state of fixed length encoded and quantized macro-blocks when quantization steps are determined by a first quantization step decision means of the encoder.

Fig.5 illustrate the state of fixed length encoded and quantized macro-blocks when the quantization steps are determined by a second quantization step decision means of the encoder.

Fig.6 is a flow chart for illustrating the process of determining the quantization step by the first quantization step decision means and the second quantization step decision means.

Fig.7 illustrates the construction of a video segment.

Fig.8 illustrates the construction of each sync block of the above-mentioned video segment.

Fig.9 illustrates the construction of the discrimination code of the sync block.

Fig.10 illustrates the construction of DCT blocks of the luminance data, R-Y data and R-B data in the sync block.

Referring to the drawings, preferred embodiments of the present invention will be described in detail.

The digital video signal recording method is carried out by a recording method for digital video signals having an encoder configured as shown in Fig.1.

That is, the encoder has a transform unit 1 for processing macro-blocks of the digital video signals with discrete cosine transform (DCT), an encoding unit 2 and a framing unit 3. The encoding unit 2 is configured for quantizing DCT coefficients resulting from DCT with a quantization step determined on the macro-block basis by shifting the quantization step determined on the basis of units each made up of plural macro-blocks.

The transform unit 1 includes a blocking circuit 11 for dividing the digital video signals into 8x8-pixel blocks, a shuffling circuit 12 for effecting macro-block based shuffling, a motion detection circuit 13, a DCT circuit 14 for effecting two-dimensional DCT with the block size of 8x8, a picture memory 15 and an activity detection circuit 16.

The encoding unit 2 includes a data quantity estimating circuit 21, a Huffman table 22 for effecting variable length coding, a first quantization step decision circuit 23, a second quantization step decision circuit 24, a quantization circuit 25 and a variable length encoding circuit 26. The data quantity estimating circuit calculates the data quantity following quantization, and the first quantization step decision circuit 23 determines the quantization step within a range of a pre-set quantity of quantized data in terms of units each consisting of five macro-blocks. The second quantization step decision circuit 24 determines the quantization steps within a range of a pre-set quantity of quantized data in terms of macro-units. The quantization circuit 25 effects quantization with quantization steps determined by the first quantization step decision circuit 23 and the second quantization step decision circuit 24. The variable length encoding circuit 26 variable length encodes the quantized data from the quantization circuit 25. The framing circuit 3 has a deshuffling circuit 31, a parity appending circuit 32 and a channel encoding circuit 33.

The processing performed by the transform unit 1 is explained.

The blocking circuit 11, fed with input digital video data, forms DCT blocks, each consisting of an array of 8x8 pixels, totalling 64 pixels, from luminance data Y, data C_R and data C_B of the same domain. The data C_R is the color difference data R-Y, while the data C_B is the color difference data B-Y. That is, the blocking circuit forms one macro-block from six DCT blocks of luminance data Y, one DCT block of color difference data C_R and one DCT block of color difference data C_B, and outputs the resulting macro-block.

The shuffling circuit 12 effects pre-set macro-block based shuffling on the digital video signals macro-blocked by the blocking circuit 11. After shuffling the macro-blocks, each one macro-block is taken out from each of super macro-blocks S1 to S5 which are separated from one another on a picture P and which are made up each of 27 macro-blocks, as shown in Fig.2. Thus, five macro-blocks M_1 to M_5 are collected to form a sole fixed length forming unit, which is outputted. The fixed length forming unit is referred to herein simply as a unit.

The shuffling sequence in the above shuffling operation conforms to the equations

$$
Vi,\ k = \begin{cases} M(i + 4)\bmod(n),\ 2,\ k \\ M(i + 12)\bmod(n),\ 1,\ k \\ M(i + 12)\bmod(n),\ 3,\ k \\ M(i)\bmod(n),\ 0,\ k \\ (M(i + 8)\bmod(n),\ 4,\ k \end{cases}
$$

where n is the number of lines, i is the line index (i = 0 to n-1) and k is the scanning order index for respective pixels of the super blocks S_1 to S_5 (k = 0 to 26). Consequently, five macro-blocks M_1 to M_5 are selected, beginning from the macro-block at the center of the picture P shown in Fig.2, that is the macro-block M_1 of the super macro-block S_1, followed by the macro-block S_2 of the super macro-block S_5, ... the macro-block M_5 of the super macro-block M_5.

On the other hand, the macro-blocks of each of the super macro-blocks S_1 to S_5 are scanned in the sequence of the macro-block 0, macro-block 1, macro-block 2, ...macro-block 26, as shown in Fig.3.

The motion detection circuit 13 effects motion detection in terms of five macro-blocks formed into one unit by the shuffling circuit 12. The results of motion detection are fed to the DCT circuit 14, while being outputted as the subsidiary information to e.g., a reproducing system, not shown.

The DCT circuit 14 performs DCT on picture data devoid of motion, in terms DCT blocks each made of 8x8 pixels, based upon the results of detection by the motion detection circuit 13. On the other hand, the DCT circuit 14 performs DCT on sum data or differential data between fields of picture data exhibiting motion in terms of 2 DCT blocks each made up of 8x4 pixels. The DCT circuit 14 outputs dc components to the framing unit 3, while outputting ac components to the picture memory 15.

The picture memory 15 transiently stores the ac components resulting from DCT by the DCT circuit 14 in terms of units.

The activity detection unit 16 detects, as the information specifying the activity of a picture, the maximum value of the ac components resulting from DCT by the DCT circuit 14 of the one-unit data stored in the picture memory 15 and outputs the results of detection as the subsidiary information to e.g., a reproducing system, not shown.

The operation of each circuit in the encoding unit 2 is explained.

The data quantity estimation circuit 21 is responsive to the results of unit-based activity detection by the activity detection circuit 12 to classify the ac components stored in the picture memory 15 in association with the degree of quantization at the time of quantization.

In order for fixed-length picture data to be obtained on the unit basis from the variable-length encoding circuit 26 fed with the output of the quantization circuit 25, the first quantization step decision circuit 23 calculates an optimum

quantization step for the luminance data Y, color difference data C_R and the color difference data C_B, based upon the information of classification from the estimation circuit 21 and the codes in the Huffman table 22.

The second quantization step decision circuit 24 determines, from the quantization step determined on the unit basis by the first quantization step decision circuit 23, the quantization step for each of the five macro-blocks in the unit within a range lesser than targeted fixed bit length. The quantization step is determined on the macro-block basis so that priority is given a macro-block among the five macro-blocks which is located closer the center of the picture.

The quantization circuit 25 quantizes the one-unit data (ac components) stored in the picture memory 15 at a quantization step as determined by the second quantization step decision circuit 24, and transmits the resulting quantization data to the variable length encoding circuit 26.

The variable length encoding circuit 26 encodes the five macro-blocks, quantized by the quantization circuit 25, using e.g., the Huffman code, so that each macro-block is formed by 77 bytes, inclusive of the quantization step information.

The operation of determining the quantization step in the first quantization step decision circuit 23 and the second quantization step decision circuit 24 is explained in detail.

If the quantization step Q, determined on the unit basis by the first quantization step decision circuit 23, is 8 (Q = 8), the same quantization step Q_0 to Q_4 (Q_0 to Q_4 = 8) is accorded to each of the five macro-blocks MO_0 to MO_4 of the unit, to which the quantization step Q = 8 is accorded, as shown in Fig.4.

If data of the five macro-blocks are quantized with the same quantization step Q = 8, vacant regions B_{11} to B_{12}, B_{21} to B_{24}, B_{31} to B_{32} and B_{41} to B_{46} are present in the macro-blocks MO_1, MO_2, MO_3 and MO_4, respectively, as shown in Fig.4.

Since the quantization step information can be accorded to each of the macro-blocks, the second quantization step decision circuit 24 shifts the quantization steps Q_0 to Q_4 of the macro-blocks MO_0 to MO_4 shown in Fig.4 in a direction of refining the quantization degree within the range less than the target fixed bit length value.

The order of priority in shifting the quantization step is the macro-block MO_0, MO_1, ..., MO_4, thus beginning from the upper side macro-block. That is, the macro-blocks MO_0 to MO_4 are respectively associated with the macro-blocks MO_0 to MO_4 shown in Fig.2 and hence are selected beginning from the macro-block located near the center of the picture. That is, the quantization step is determined so that priority will be given the macro-blocks located closer to the center of the picture.

If the quantization step is determined on the macro-block basis in the second quantization step decision circuit 24 as described above, the quantization step Q_0 of the macro-block MO_0 becomes finer by one and is now 9 (Q_0 = 9), while the quantization step Q_1 of the macro-block MO_1 becomes finer by one and is now 9 (Q_0 = 9), as shown in Fig.5. Consequently, the vacant region comprises the vacant regions A_{31} to A_{32} of the macro-block MO_3 and the vacant regions A_{41} to A_{45} of the macro-block MO_4.

By determining the quantization step on the macro-block basis within the range of the targeted fixed bit length, redundant bits may be effectively utilized, while a picture of a high picture quality may be produced. In addition, by refining the quantization steps of the five macro-blocks in the order of the quantization steps Q_0, Q_1, ..., Q_4, the finer quantization steps are selected preferentially beginning from the central portion of the picture, so that satisfactory picture quality may be obtained at the central region of the picture which is most outstanding to the viewer.

Referring to the flow chart shown in Fig.6, the process of determining the quantization step in the first quantization step decision circuit 23 and the second quantization step decision circuit 24 is explained.

In the first quantization step decision circuit 23, the first quantization i is initialized (i = 15). The quantization steps are 0 to 15, in which the larger the number, the finer is the quantization step.

The quantization steps Q_0 to Q_4 of the five macro-blocks M_0 to MO_4 are set at step S2 to the first quantization step i ($=Q_4 = Q_3 = Q_2 = Q_1 = Q_0$).

Then, at step S3, the five macro-blocks M_0 to M_4 are quantized with the quantization step i ($=Q_4 = Q_3 = Q_2 = Q_1 = Q_0$), while the resulting quantized data is variable-length encoded using the Huffman table 22.

Then, at step S4, the first quantization step i is rendered rougher, that is decremented (i = i - 1).

It is then judged at step S5 whether the quantity of the quantized data resulting from quantization at step S3 is less than the targeted fixed bit length value, whether the quantity of the resulting quantized data is more than the targeted fixed bit length value target, or whether the quantity of the resulting quantized data is equal to the targeted fixed bit length value target.

If, as a result of judgment at step S5, the quantity of the produced quantized data exceeds the fixed length value target, processing reverts to step S2 in order to effect at step S3 the quantization with a quantization step rougher by one and in order to repeat the steps S4 and S5.

Alternatively, if the quantity of the produced quantized data is equal to the fixed length value target, the first quantization step i is set as quantization steps Q_0 to Q_4 for the macro-blocks M_0 to Q_4. The quantization steps Q_0 to Q_4 for the macro-blocks M_0 to Q_4 are then outputted to the quantization circuit 25 without performing the steps S6 ff. of determining the macro-block based quantization step determining process which is to be explained subsequently.

Alternatively, if the quantity of the produced quantized data is lower than the fixed length value target, the second quantization step decision circuit 24 initializes, at step S6, the index j (j: $0 \leq j \leq 4$) of the macro-blocks M_0 to M_4 ($j = 0$). The circuit 24 then refines at step S7 the quantization step information Q_j of the jth macro-block M_j by one ($G_j = Q_j + 1$).

At step S8, the circuit 24 then quantizes the macro-block M_j with the quantization step Q_j determined at the step S7, while variable length encoding the quantized data using the Huffman table 22.

It is then judged at step S9 whether the quantity of the quantized data resulting from quantization at step S8 is less than the targeted fixed length value, whether the quantity of the resulting quantized data is more than the targeted fixed length value or whether the quantity of the resulting quantized data is equal to the targeted fixed length value.

If, as a result of judgment at step S9, the quantity of the quantized data is less than the fixed length value target, the index is advanced at step S10 to the next macro-block $M_{j=j+1}$ in order to revert to the processing at step S7 and in order to repeat the step S7 ff.

Alternatively, if the quantity of the resulting quantized data is equal to the fixed length value target, the quantization step information of the macro-block M_j is set as the second quantization step Q_j in order to output the quantization steps Q_0 to Q_4 for the macro-blocks M_0 to Q_4 to the quantization circuit 25.

Alternatively, if the quantity of the resulting quantized data exceeds the fixed length value target, the quantization step information of the macro-block M_j is decremented by one in order to set at step S11 the quantization step information for the macro-block M_j as the quantization step Q_j (= Q_j - 1) and in order to output the quantization steps Q_0 to Q_4 for the macro-blocks M_0 to M_4 to the quantization circuit 25.

The quantization steps are determined on the macro-block basis by the first quantization step decision circuit 23 and the second quantization step decision circuit 24 as described above in order to carry out the quantization with the quantization step as determined by the quantization circuit 25. The variable length encoding circuit 26 adds the quantization step information to the quantized data on the macro-bloc basis as shown in Figs.4 and 5 and forms fixed bit length codes which are outputted to the framing unit 3.

The quantization steps determined by the first quantization step decision circuit 23 and the second quantization step decision circuit 24 are also supplied as the subsidiary information to the reproducing system, not shown.

The processing by the respective components of the framing unit 3 is now explained.

The deshuffling circuit 31 deshuffles the dc components from the DCT circuit 14 and the ac components quantized with the quantization step accorded on the macro-block basis by the variable length encoding circuit 26 and re-arrays the macro-blocks in a continuous sequence on the picture.

The parity appending circuit 32 appends the synchronization codes $sync_0$ to $sync_4$, identification codes ID_0 to ID_4 and parities P_0 to P_4 in order to constitute sync blocks SB_0 to SB_4 making up one video segment.

That is, referring to Fig.8, each sync block is made up of 90 bytes, i.e., 16-bit or 2-byte synchronization code sync as an area for recognition of the leading end of the sync by two sync patterns, 3-byte identification codes IDO to ID2, 77-byte sync block SB fixed in bit length and quantized as described above and 8-byte parity P as error correcting parity data.

As for the identification codes IO to I2, the identification code I0 is made up of a sequence number SNo, while the identification codes I1 and I2 are constituted by a sync block number SBNo and an application number ANo, respectively as shown in Fig.9.

Each of the luminance data Y and the color difference data C_R, C_B, shown in Fig.7, is made up of a 9-bit dc component, a 1-bit mode data mo specifying one of 8x8/2x4x8 block sizes used for DCT by the DCT circuit 13, the classification information c1 obtained by the data quantity estimation circuit 21 and the fixed-length ac component of luminance data (for luminance data Y) or of color difference data (for the color difference data C_R and C_B), as shown in Fig.10.

The ac component of the luminance data Y is made up of 68 bits, while the ac components of the color difference data C_R, C_B are each made up of 52 bits.

The sync blocks SB_0 to SB_4, having the parity codes appended thereto, are supplied as one video segment to the channel coding circuit 33. The video segment is channel-coded by the channel coding circuit 33 so as to be recorded at pre-set positions on a magnetic tape by recording means, not shown.

The operation of the encoder shown in Fig.1 is explained.

The blocking circuit 11 divides video signals, converted into digital signals, into DCT blocks each made up of 8x8 pixels, totalling 64 pixels, and forms a macro-block from six DCT blocks of luminance data, one DCT block of color difference data C_R and one DCT block of color difference data C_B, totalling eight DCT blocks, in order to output the resulting macro-block to the shuffling circuit 12.

The shuffling circuit 12 shuffles the macro-blocked video signals from the blocking circuit 11 and collects five macro-blocks into one unit which is outputted to the DCT circuit 14 and the motion detection circuit 13. The also unit is referred to herein as unit data.

The motion detection circuit 13 detects the motion of the unit data from the shuffling circuit 12 and outputs the results of detection to the DCT circuit while outputting the same results to the reproducing side as the subsidiary information.

The DCT circuit 14 performs two-dimensional DCT on unit data from the shuffling circuit 12 while selectively switching

between the intra-frame pixel values for the 8X8 pixel block unit and inter-field prediction error values 4X8X2 for the pixel block unit by way of performing two-dimensional DCT. The dc components are fed to the deshuffling circuit 31 of the framing unit 3, while the ac components are fed to the picture memory 15 and to the activity detection circuit 16.

The picture memory 15 stores the ac components from the DCT circuit 14.

The activity detection circuit 16 detects the picture activity for the ac components from the DCT circuit 14 and outputs the results of detection to the data quantity estimating circuit 21 of the encoding unit 2 while outputting the same results to the reproducing side as the subsidiary information.

The data quantity estimating circuit 21 classifies the ac components in association with the degree of quantization responsive to the results of detection from the activity detection circuit 12. The classified data is supplied to the first quantization step decision circuit 23.

The first quantization step decision circuit 23 calculates an optimum quantization step for the unit data within a range smaller than the targeted fixed bit length value based upon the classification data from the data quantity estimation circuit 21 and the codes from the Huffman table 22. The calculated quantization step is sent to the second quantization step decision circuit 24.

The second quantization step decision circuit 24 determines the quantization step on the macro-block basis within the range of less than the target fixed bit length value, based upon the quantization step for the unit data supplied from the first quantization step decision circuit 23, while giving priority to the macro-block among the five macro-blocks in the unit data which is located closer to the picture center. The quantization step determined on the macro-block basis is supplied to the quantization circuit 25, while being outputted as the subsidiary information to the reproducing side.

The quantization circuit 25 quantizes the ac components for the unit data stored in the picture memory 15 with the quantization step for the respective macro-blocks from the second quantization step decision circuit 24, and transmits quantized ac components to the variable length encoding circuit 26.

The variable length encoding circuit 26 encodes the quantized ac components from the quantization circuit 25 on the macro-block basis and transmits the encoded ac components to the deshuffling circuit 31 of the framing unit 3.

The deshuffling circuit 31 deshuffles the dc components from the DCT circuit 14 and the quantized and encoded ac components from the variable length encoded ac components and re-arrays the data so that the five macro-blocks of the unit data will be continuous on the picture. The deshuffled five macro-blocks are sent to the parity appending circuit 32.

The parity appending circuit 32 appends parity codes etc. to the five macro-blocks from the deshuffling circuit 31 to form a sync block from the macro-blocks having the parity codes etc. and forms a video segment from the five sync blocks. The resulting video segment is sent to the channel coding circuit 33.

The video segment is channel-coded by the channel coding circuit 33 so as to be transmitted to a recording unit, not shown.

Claims

1. A method for recording quantized and encoded digital video signals comprising the steps of:
   determining a quantization step in terms of a video segment made up of plural macro-blocks as a unit so that the quantity of quantized data is less than a pre-set data quantity;
   determining a quantization step in terms of the macro-blocks as a unit so that the quantity of quantized data is less than the pre-set data quantity; and
   quantizing the digital video signals with the determined quantization steps.

2. The method as claimed in claim 1, wherein the quantization step is determined on the macro-block basis by giving priority to the macro-block which is located at a mid portion of a picture.

3. The method as claimed in claim 1, wherein the number of the macro-blocks in the video segment is five.

4. The method as claimed in claim 1, wherein the first quantization step decision means calculates the optimum quantization step for each of the luminance signals and color signals of the video signals by arithmetic operations.

5. An apparatus for recording quantized and encoded digital video signals comprising:
   first quantization step decision means for determining a quantization step in terms of a video segment made up of plural macro-blocks as a unit so that the quantity of quantized data is less than a pre-set data quantity;
   second quantization step decision means for determining a quantization step in terms of the macro-blocks as a unit so that the quantity of quantized data is less than a pre-set data quantity; and
   quantization means for quantizing the digital video signals with the quantization steps determined by said first

quantization step decision means and said second quantization step decision means.

6. The apparatus as claimed in claim 5 wherein the quantization step is determined on the macro-block basis by giving priority to the macro-block which is located at a mid portion of a picture.

7. The apparatus as claimed in claim 6, wherein the number of the macro-blocks in the video segment is five.

8. The apparatus as claimed in claim 7, wherein the first quantization step decision means calculates the optimum quantization step for each of the luminance signals and color signals of the video signals by arithmetic operations.

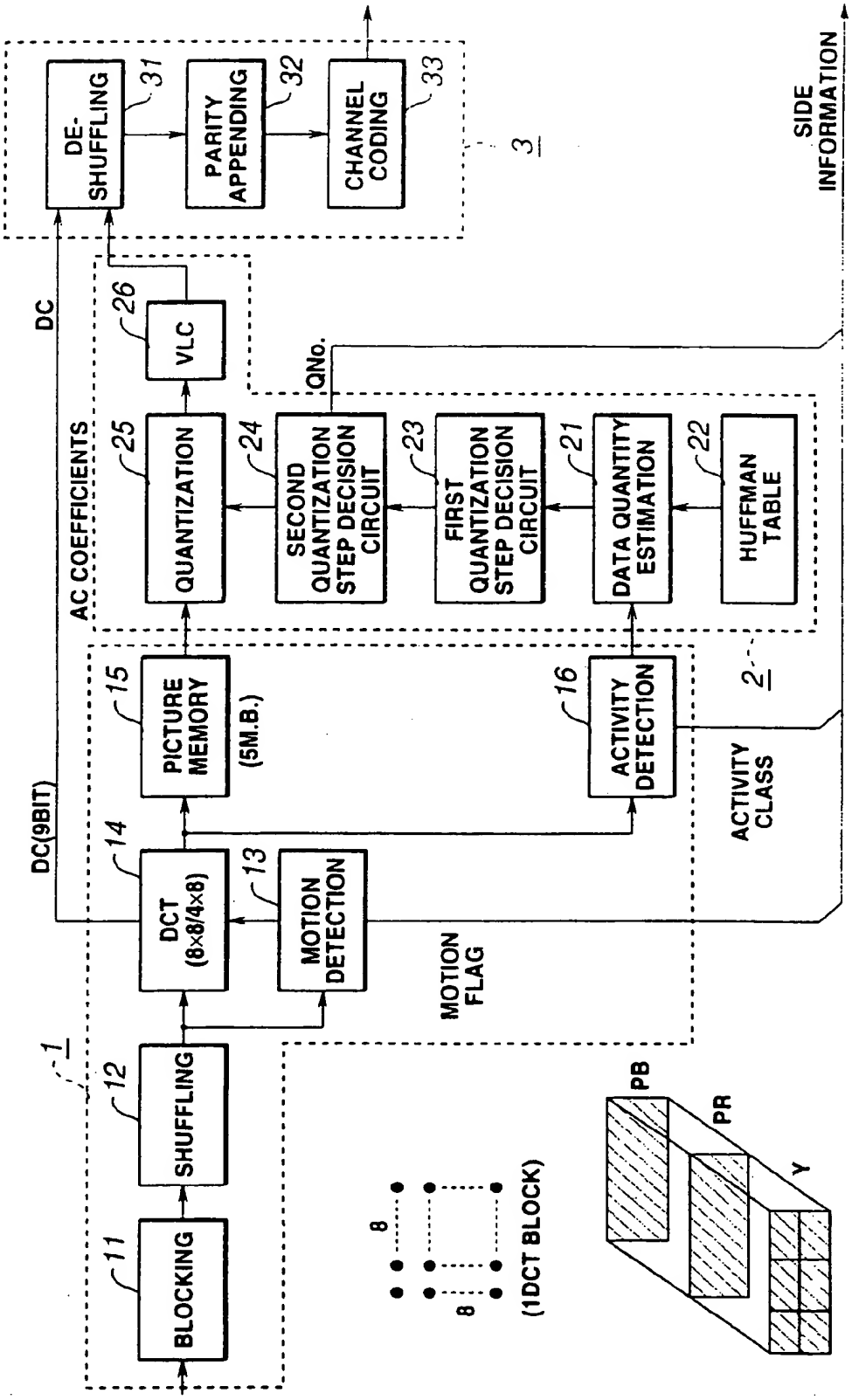

1
2
3
BLOCKING
11
SHUFFLING
12
DCT (8×8/4×8)
14
MOTION DETECTION
13
PICTURE MEMORY
15
(5M.B.)
ACTIVITY DETECTION
16
DC(9BIT)
DC
AC COEFFICIENTS
MOTION FLAG
ACTIVITY CLASS
QUANTIZATION
25
SECOND QUANTIZATION STEP DECISION CIRCUIT
24
FIRST QUANTIZATION STEP DECISION CIRCUIT
23
DATA QUANTITY ESTIMATION
21
HUFFMAN TABLE
22
VLC
26
QNo.
DE-SHUFFLING
31
PARITY APPENDING
32
CHANNEL CODING
33
SIDE INFORMATION
8
8
(1DCT BLOCK)
PB
PR
Y

FIG.1

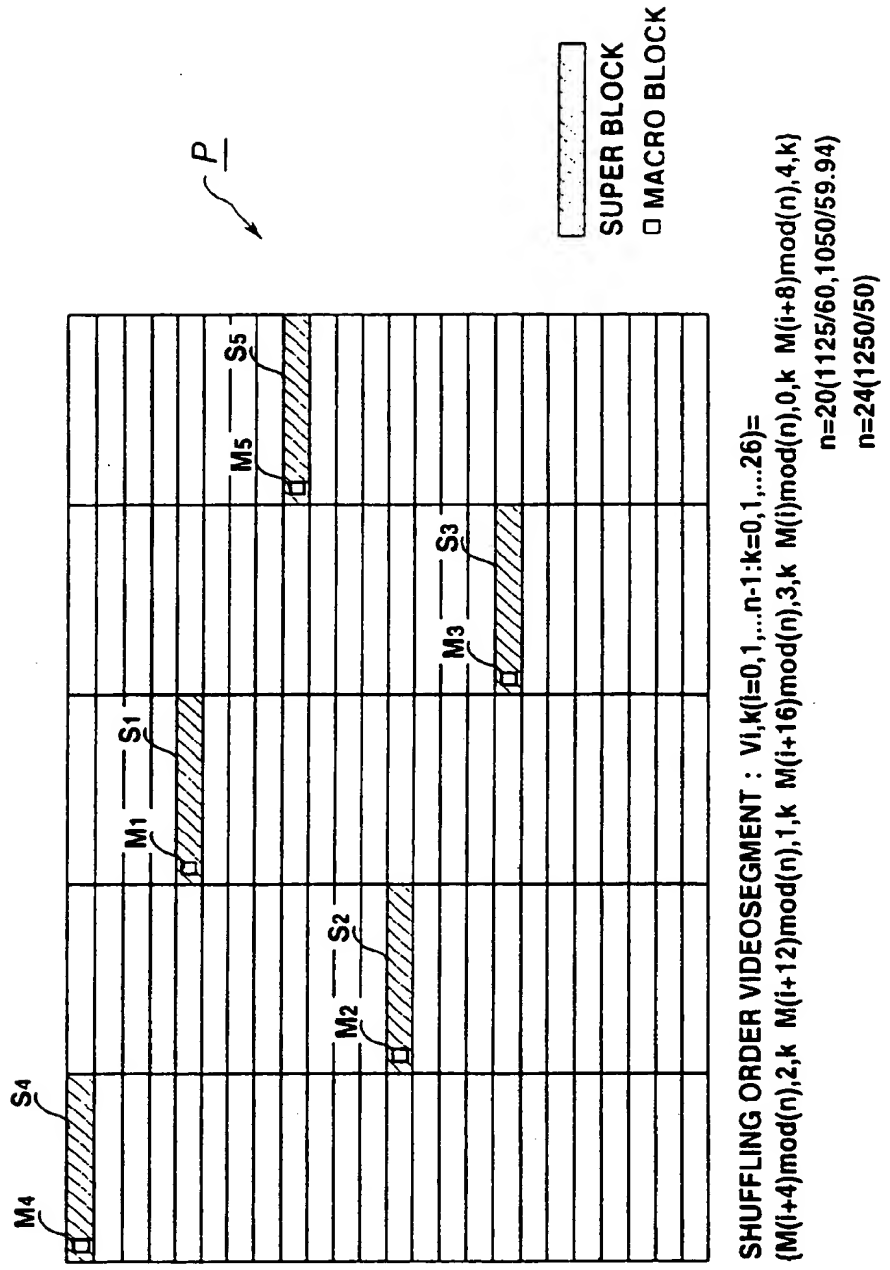
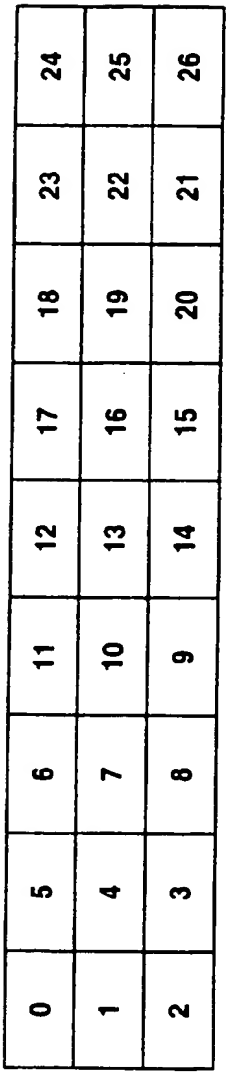

P
SUPER BLOCK
MACRO BLOCK
M1
S1
M2
S2
M3
S3
M4
S4
M5
S5
SHUFFLING ORDER VIDEOSEGMENT : Vl,k(i=0,1,...n-1:k=0,1,...26)=
{M(i+4)mod(n),2,k M(i+12)mod(n),1,k M(i+16)mod(n),3,k M(i)mod(n),0,k M(i+8)mod(n),4,k}
n=20(1125/60,1050/59.94)
n=24(1250/50)

FIG.2



MACRO BLOCK ONE SUPER BLOCK $S_{i,j}$: $MI_{i,j,k}$ (k=0,1,...26) (j=0,1,...4) (i=0,1,...19) FOR 1125/60
(i=0,1,...23) FOR 1150/50

FIG.3

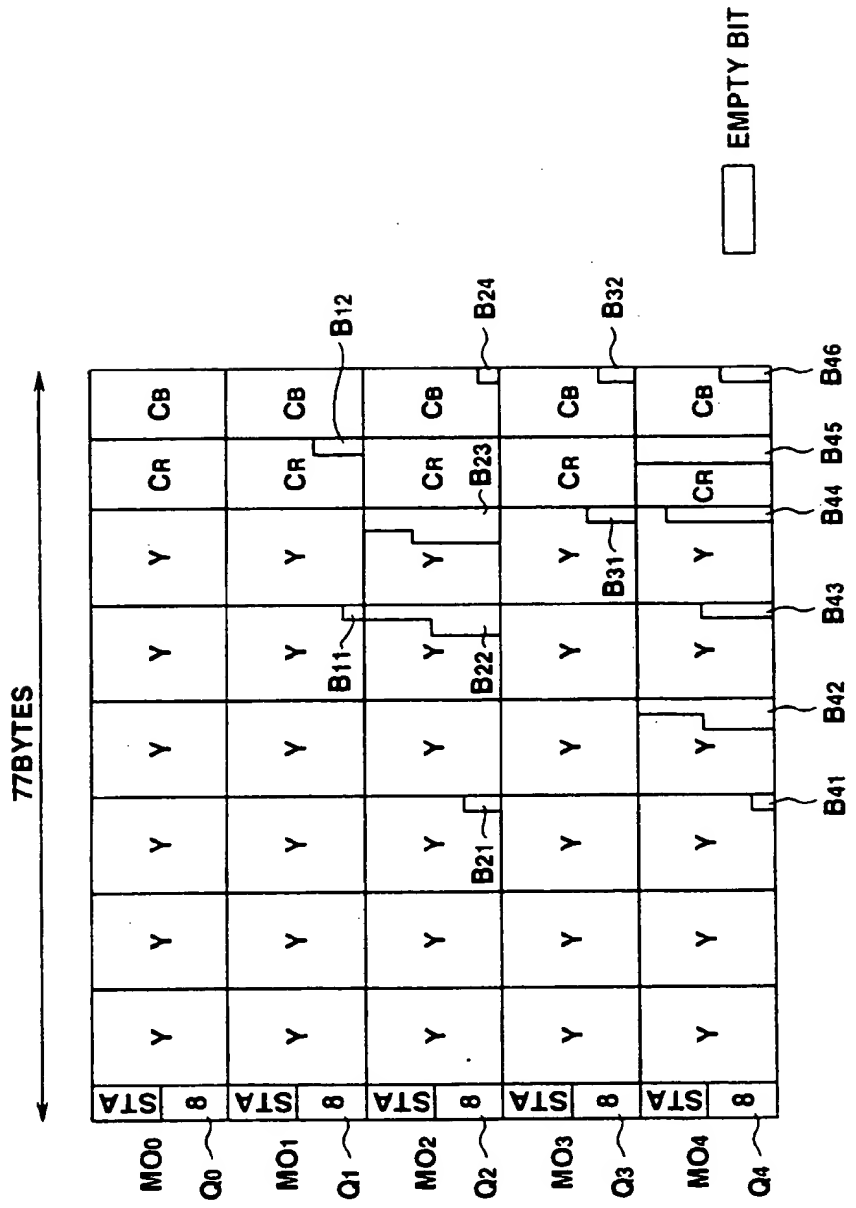

EMPTY BIT
77BYTES
MO0
MO1
MO2
MO3
MO4
Q0
Q1
Q2
Q3
Q4
STA
8
Y
CR
CB
B11
B12
B21
B22
B23
B24
B31
B32
B41
B42
B43
B44
B45
B46

FIG.4

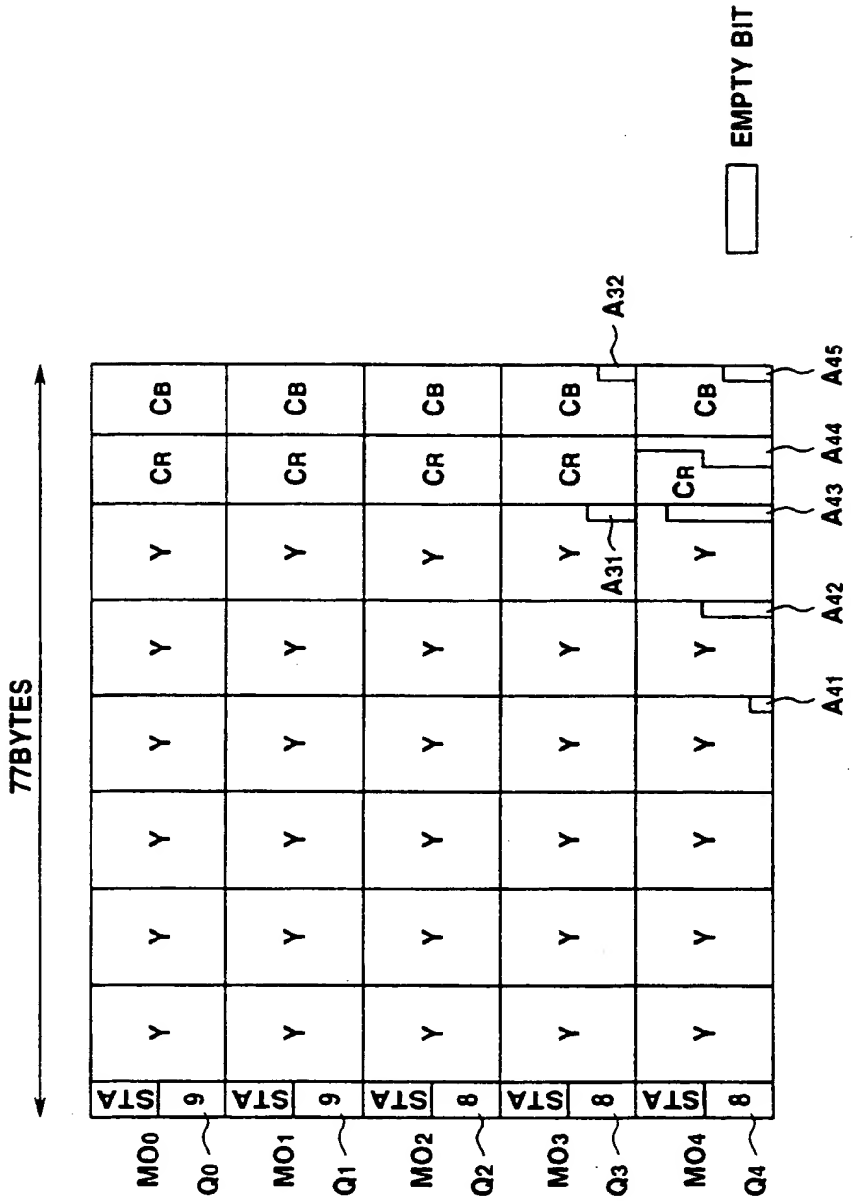

EMPTY BIT
77BYTES
MO0
Q0
MO1
Q1
MO2
Q2
MO3
Q3
MO4
Q4
STA
CB
CR
Y
A31
A32
A41
A42
A43
A44
A45

FIG.5

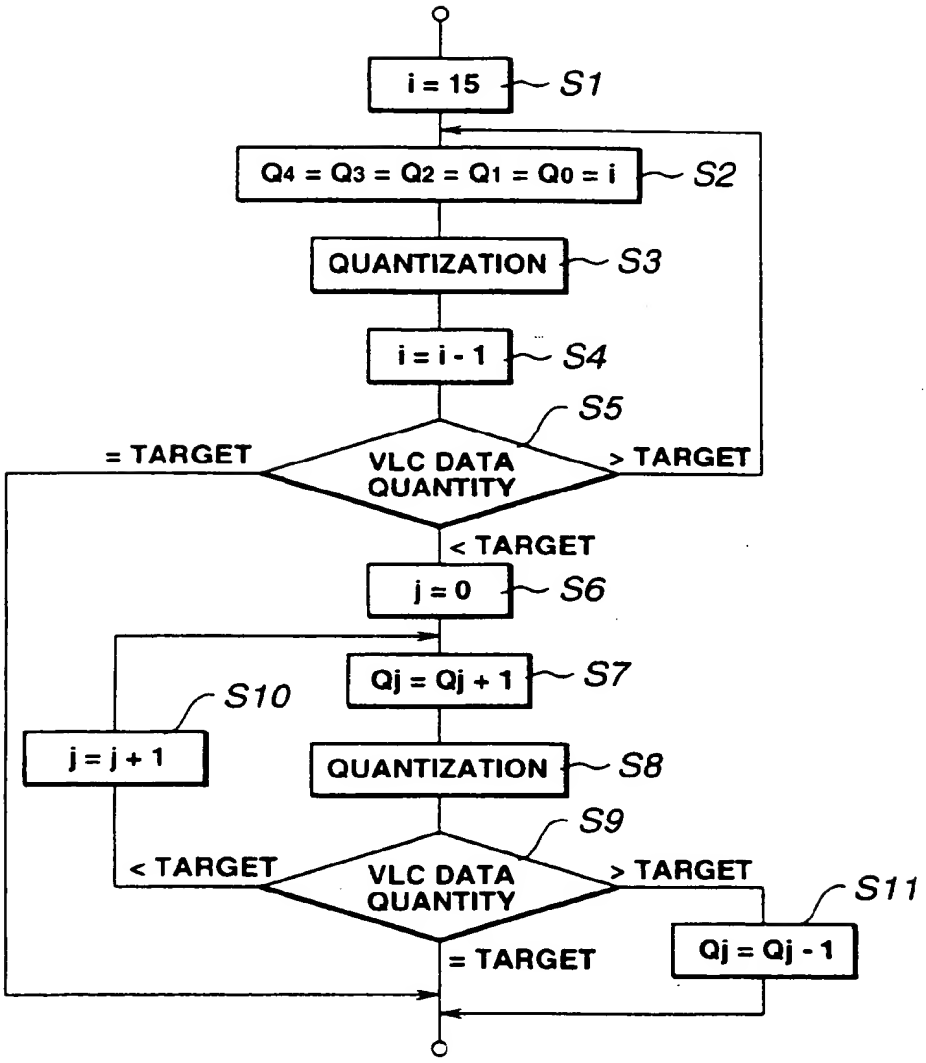
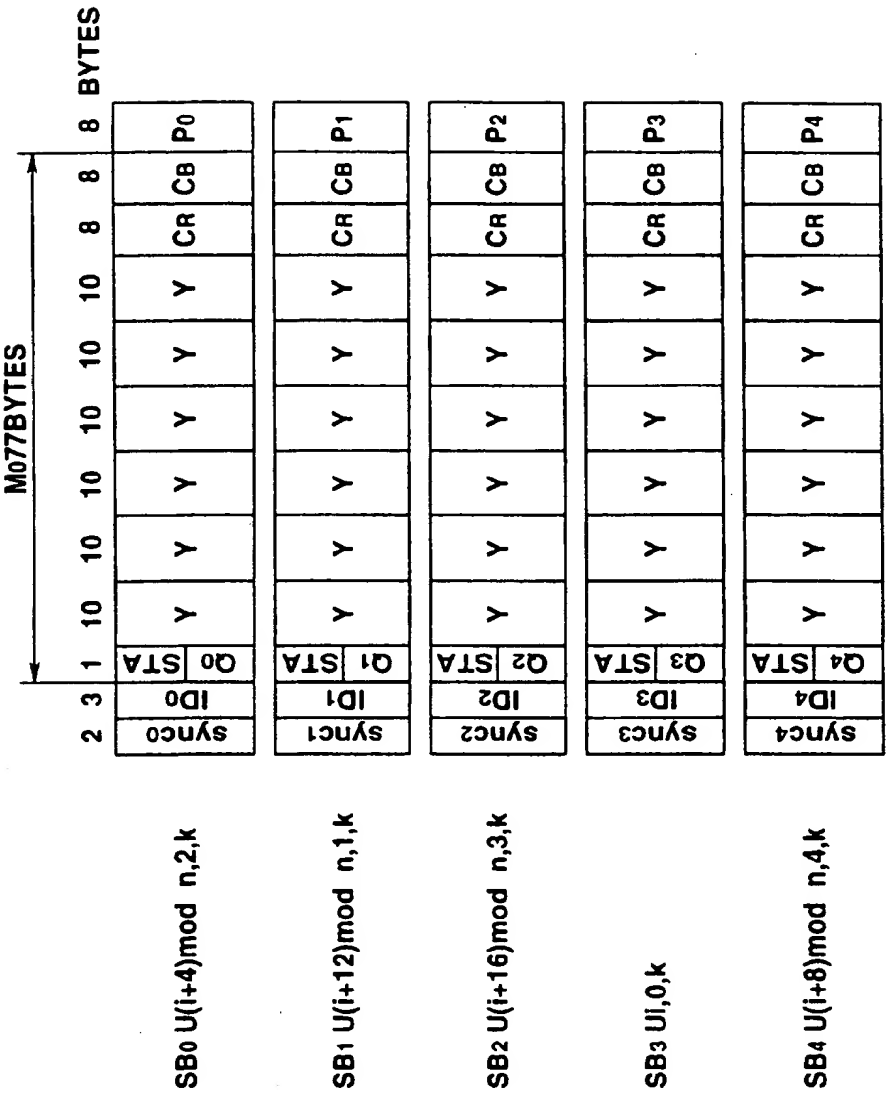

i = 15
S1
Q4 = Q3 = Q2 = Q1 = Q0 = i
S2
QUANTIZATION
S3
i = i - 1
S4
S5
= TARGET
VLC DATA QUANTITY
> TARGET
< TARGET
j = 0
S6
Qj = Qj + 1
S7
S10
j = j + 1
QUANTIZATION
S8
S9
< TARGET
VLC DATA QUANTITY
> TARGET
S11
= TARGET
Qj = Qj - 1

FIG.6



One unit Ui,j,k(sync block) includes all part of most part of one macro block Mi,j,k.

- STA : 4bits indicate the concealment information.
- QN0.: 4bits indicate the quantize number of quantization strategy.

FIG.7

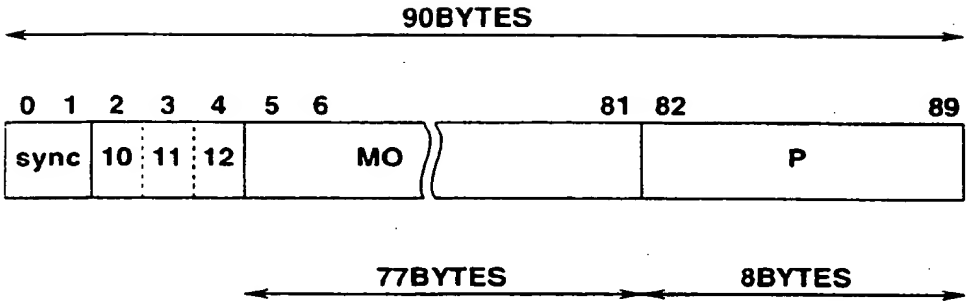


FIG.8

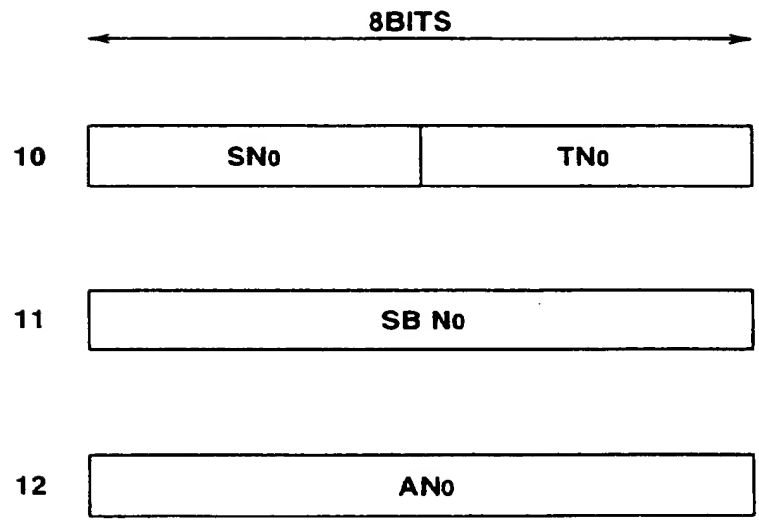
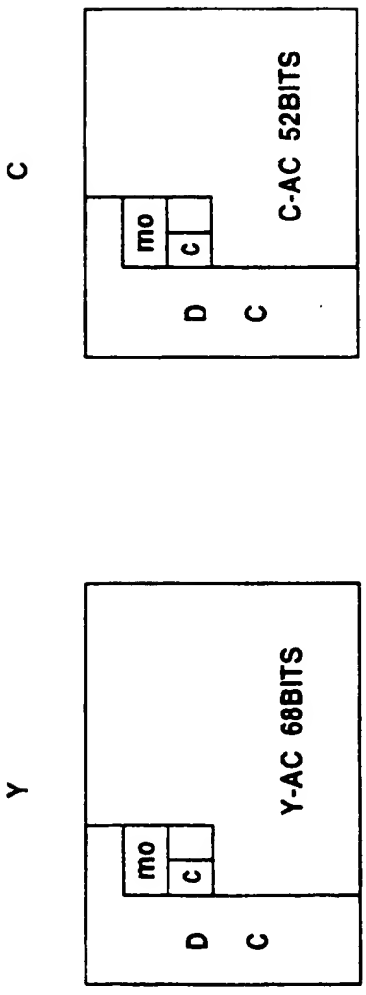


FIG.9



· DC : 9bits of DC coefficient.
· mo : One bit indicates the mode information of DCT.(8×8/2×4×8)
· cl : 2bits indicate the class number.

FIG.10

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 697 792 A3

(12) EUROPEAN PATENT APPLICATION

(88) Date of publication A3:
22.10.1997 Bulletin 1997/43

(43) Date of publication A2:
21.02.1996 Bulletin 1996/08

(21) Application number: **95305784.1**

(22) Date of filing: **18.08.1995**

(51) Int Cl.[6]: **H04N 5/92**, H04N 7/30, H04N 7/54, H04N 9/804, H04N 7/26, H04N 7/36

(84) Designated Contracting States:
AT DE FR GB IT NL

(30) Priority: **19.08.1994 JP 195230/94**

(71) Applicant: **SONY CORPORATION**
Tokyo (JP)

(72) Inventors:
- **Oikawa, Yuka, c/o Int. Prop. Div. Sony Corp.**
  Shinagawa-ku, Tokyo 141 (JP)
- **Yanagihara, Naofumi,**
  c/o Int. Prop. Div. Sony Corp
  Shinagawa-ku, Tokyo 141 (JP)
- **Izumi, Nobuaki, c/o Int. Prop. Div. Sony Corp**
  Shinagawa-ku, Tokyo 141 (JP)

(74) Representative: **Cotter, Ivan John et al**
D. YOUNG & CO.
21 New Fetter Lane
London EC4A 1DA (GB)

(54) Recording digital video signals

(57) In a technique for recording digital video signals, digital video signals in the form of DCT coefficients, obtained by e.g. discrete cosine transformation, are quantized and compressed so as to be recorded on a recording medium. A first quantization step decision unit (23) determines a quantization step in terms of a video segment made up of plural macro-blocks as a unit so that the quantity of quantized data is less than a pre-set data quantity. A second quantization step decision unit (24) determines a quantization step in terms of the macro-blocks as a unit so that the quantity of quantized data is less than the pre-set data quantity. A quantization unit (25) quantizes the digital video signals with quantization steps determined by the first and second quantization step decision units (23, 24). This enables efficient encoding and improved picture quality.

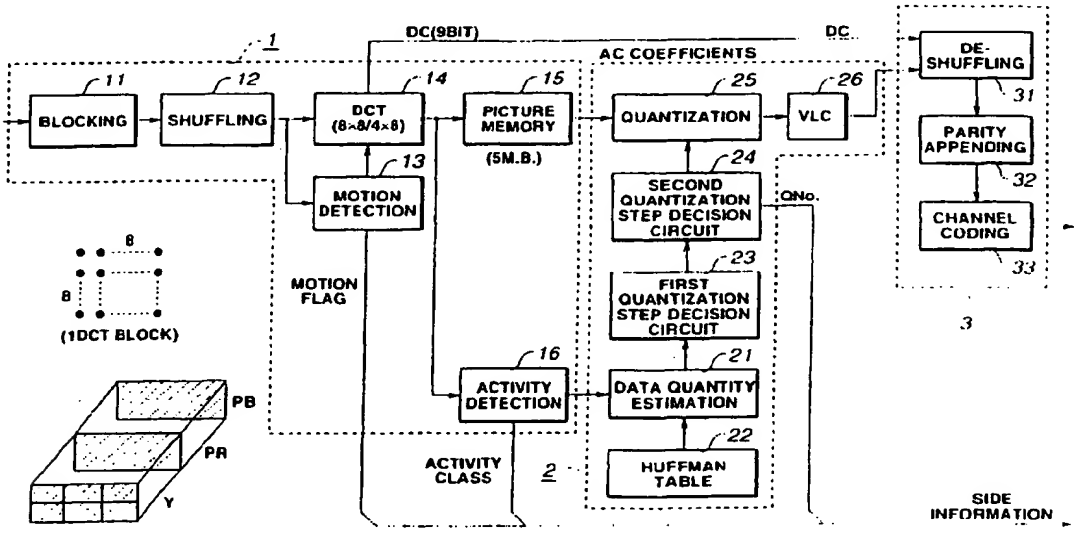


FIG.1

EP 0 697 792 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 95 30 5784

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	EP 0 401 854 A (MATSUSHITA ELECTRIC IND CO LTD) 12 December 1990	1,5	H04N5/92 H04N7/30
Y	* page 12, line 11 - line 20; figure 29 *	2-4,6-8	H04N7/54
	* page 5, line 24 - line 33; figure 7 *		H04N9/804 H04N7/26
Y	EP 0 554 871 A (SONY CORP) 11 August 1993	2-4,6-8	H04N7/36
A	* page 4, line 22 - line 31 *	1,5	
	* page 6, line 28 - line 30 *		
	* page 9, line 18 - line 23 *		
	* figures 6,10 *		
X	EP 0 540 961 A (IBM) 12 May 1993	1,5	
	* page 14, line 11 - line 37 *		
X	EP 0 470 773 A (MATSUSHITA ELECTRIC IND CO LTD) 12 February 1992	1,5	
A	* page 13, line 5 - line 15; figure 24 *	2-4,6-8	
E	EP 0 677 968 A (MATSUSHITA ELECTRIC IND CO LTD) 18 October 1995	1,3,4	
	* column 4, line 36 - column 5, line 19 *		
	* column 7, line 35 - column 8, line 5 *		
	* column 17, line 48 - line 55; figure 10 *		
X	IEEE TRANSACTIONS ON CONSUMER ELECTRONICS, vol. 39, no. 3, 1 August 1993, pages 545-554, XP000396331 LIANG-WEL LEE ET AL: "ON THE ERROR DISTRIBUTION AND SCENE CHANGE FOR THE BIT RATE CONTROL OF MPEG"	1,5	
A	* abstract *	2-4,6-8	
	* paragraph II *		
A	EP 0 385 654 A (SONY CORP) 5 September 1990	1,5	
	* abstract; figures 2,11 *		

TECHNICAL FIELDS SEARCHED (Int.Cl.6)
H04N

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	29 August 1997	Berbain, F

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)